

## MMG-202543-M5 20 Watt 2.0 - 2.5 GHz GaN Power Amplifier

### FEATURES

- Psat: +44dBm
- PAE: >50%
- Power Gain @ Psat: 24dB
- Small Signal Gain: 27dB
- QNF Package: 5.0 mm x 5.0 mm

Testing conditions: Pulsed RF signal with 1ms pulse width and 20% duty cycle

### DESCRIPTION

The MMG-202543-M5 is a high-performance Gallium Nitride (GaN) MMIC power amplifier in a QFN package with high reliability. The MMG-202543-M5 provides >20W of saturated output power, >50% power-added efficiency, and 24 dB of large-signal gain between 2.0 GHz and 2.5 GHz. Both input and output are matched to 50 ohms. Ideal applications include wireless mesh networks, Point-to-point wireless data links, military wireless communications, telemetry, and avionics.

### TYPICAL RF PERFORMANCE

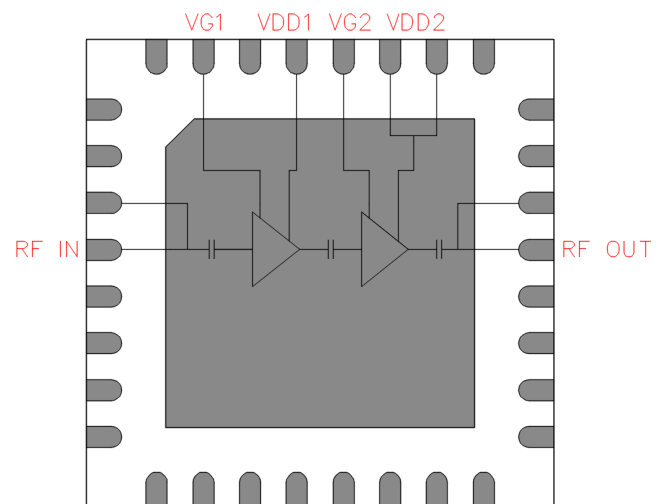
$VDD1 = 12V$ ,  $VDD2 = 28V$ ,  $IDQ1 = 34mA$ ,  $IDQ2 = 100mA$ ,  $VG1 = -2.45V$ ,  $VG2 = -2.45V$ ,  $Ta = 25\text{ }^{\circ}\text{C}$ ,  $Z0 = 50\text{ohm}$

| PARAMETER                    | UNITS                       | TYPICAL            |
|------------------------------|-----------------------------|--------------------|
| Frequency Range              | GHz                         | 2 - 2.5            |
| Gain                         | dB                          | 27                 |
| Gain Flatness                | +/-dB                       | 0.7                |
| Input Return Loss            | dB                          | 7                  |
| Output Return Loss           | dB                          | 12                 |
| Output Psat (2.0 - 2.3 GHz)  | dBm                         | 45                 |
| Output Psat (2.4 - 2.5 GHz)  | dBm                         | 44                 |
| PAE (2.0 - 2.3 GHz)          | %                           | 48                 |
| PAE (2.4 - 2.5 GHz)          | %                           | 65                 |
| EVM @ Pout of 37dBm or below | %                           | < 5                |
| Operating Current Range      | mA                          | See plot on page 2 |
| Thermal Resistance           | $^{\circ}\text{C}/\text{W}$ | 4                  |

### APPLICATIONS

- Wireless Mesh Networks
- Point-to-Point Microwave Data Links
- Military Wireless Communications
- Telemetry
- Avionics

### FUNCTIONAL DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

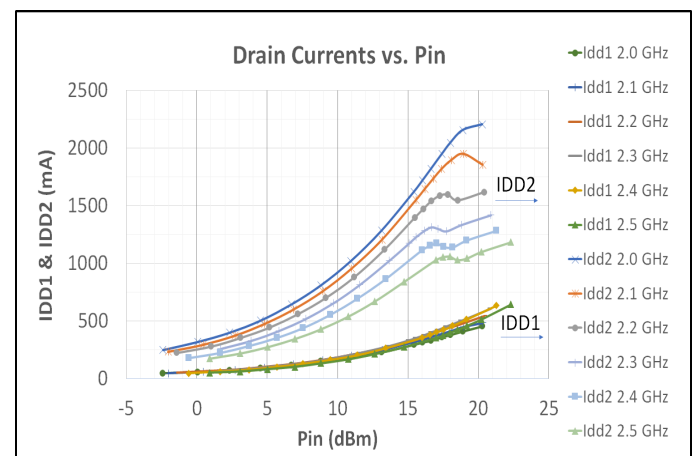
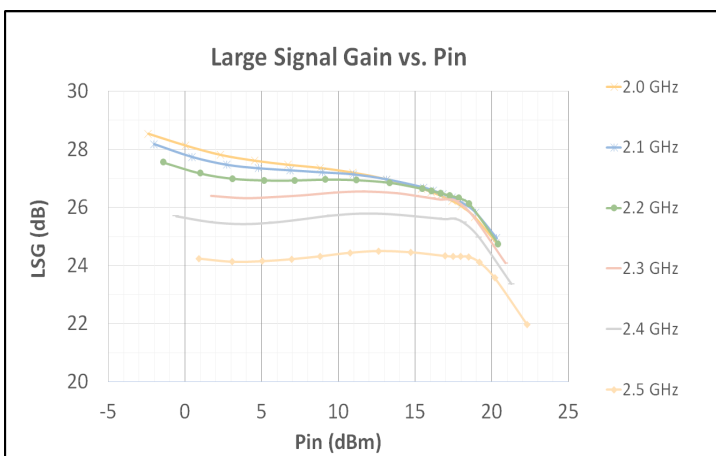
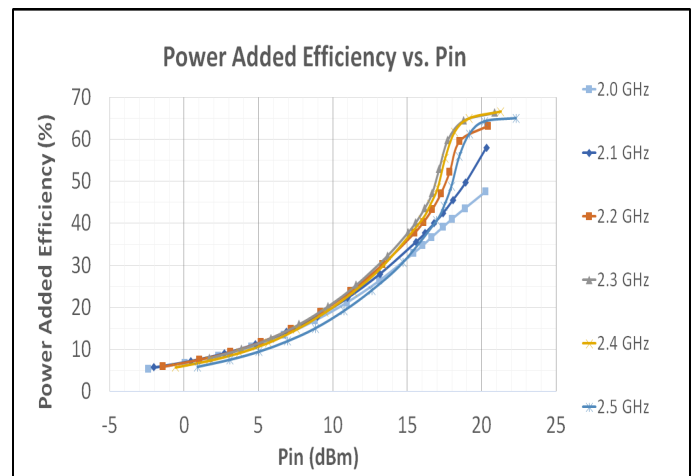
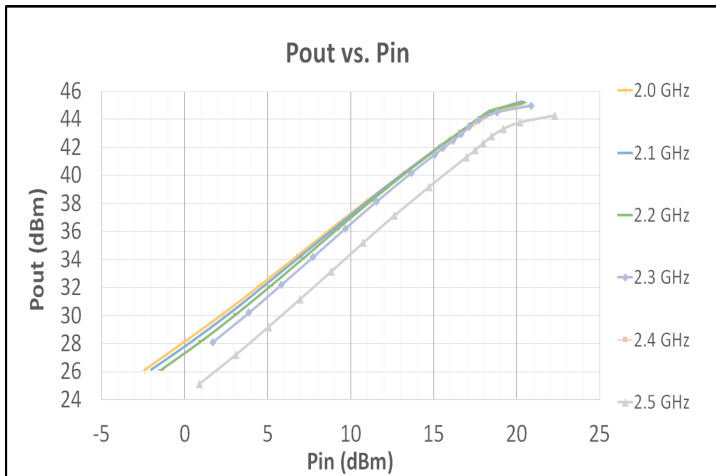
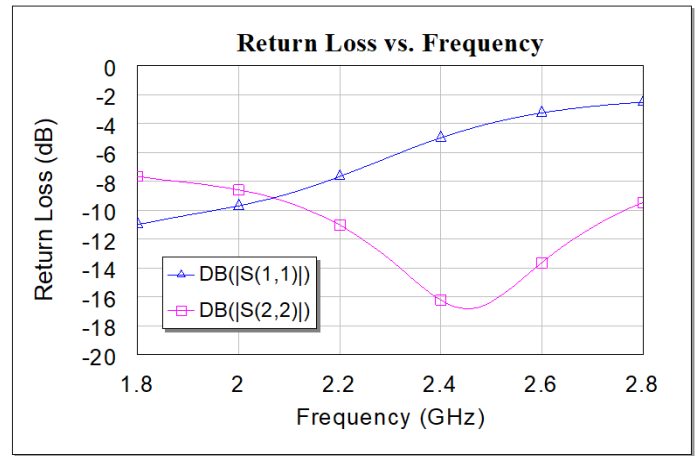
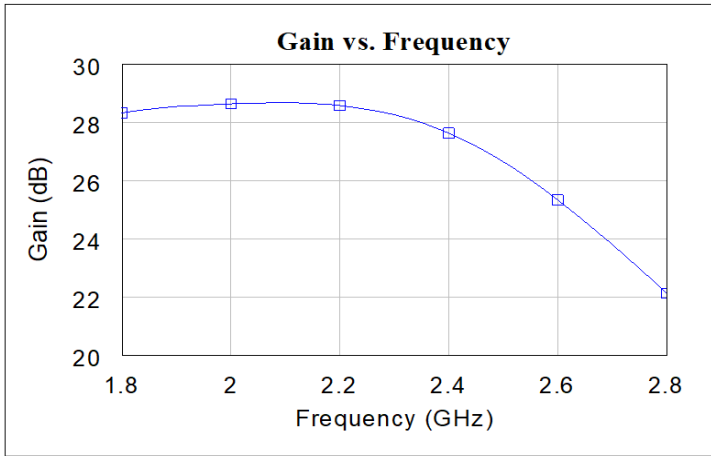
$Ta = 25\text{ }^{\circ}\text{C}$

| SYMBOL  | PARAMETERS                 | UNITS              | MAX        |
|---------|----------------------------|--------------------|------------|
| Vds     | Drain to Source Voltage    | V                  | 50         |
| Vgs     | Gate to Source Voltage     | V                  | 10         |
| Idd1    | Drain Current of 1st Stage | mA                 | 800        |
| Idd2    | Drain Current of 2nd Stage | mA                 | 1500       |
| Ig1     | Gate Current of 1st Stage  | mA                 | 3          |
| Ig2     | Gate Current of 2nd Stage  | mA                 | 6          |
| Pdiss   | DC Power Dissipation       | W                  | 46         |
| Pin max | Max RF Input Power         | dBm                | +22        |
| Tch     | Channel Temperature        | $^{\circ}\text{C}$ | 210        |
| Tstg    | Storage Temperature        | $^{\circ}\text{C}$ | -55 to 150 |

Exceeding any of these limits may cause permanent damage.

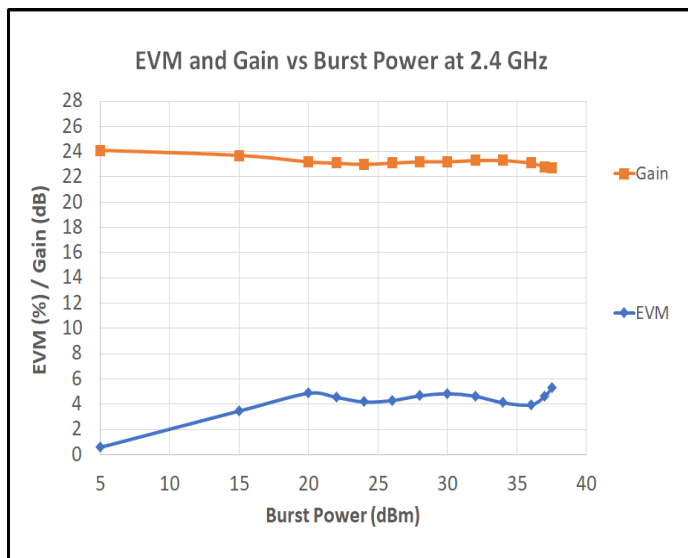
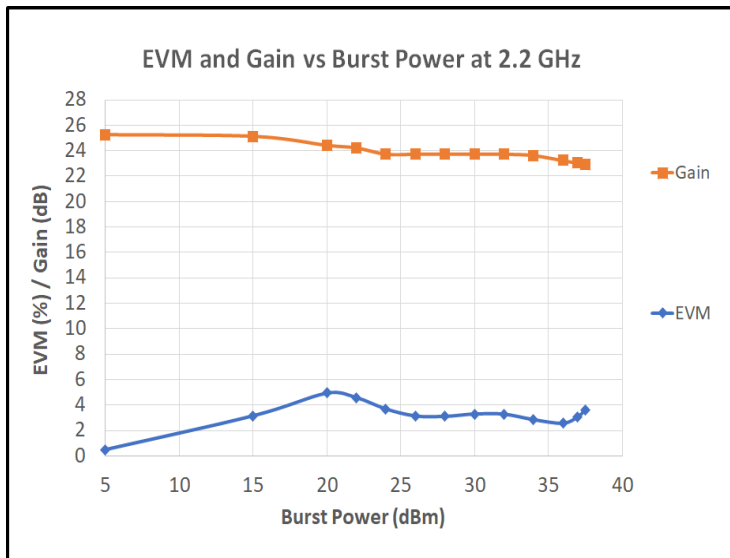
### TYPICAL RF PERFORMANCE

Test conditions unless otherwise noted:  $VDD1 = 12V$ ,  $VDD2 = 28V$ ,  $VG1 = -2.45V$ ,  $VG2 = -2.45V$ ,  $IDQ1 = 34mA$ ,  $IDQ2 = 100mA$ ,  $T_a = 25^\circ C$ ,  $Z_0 = 50\Omega$

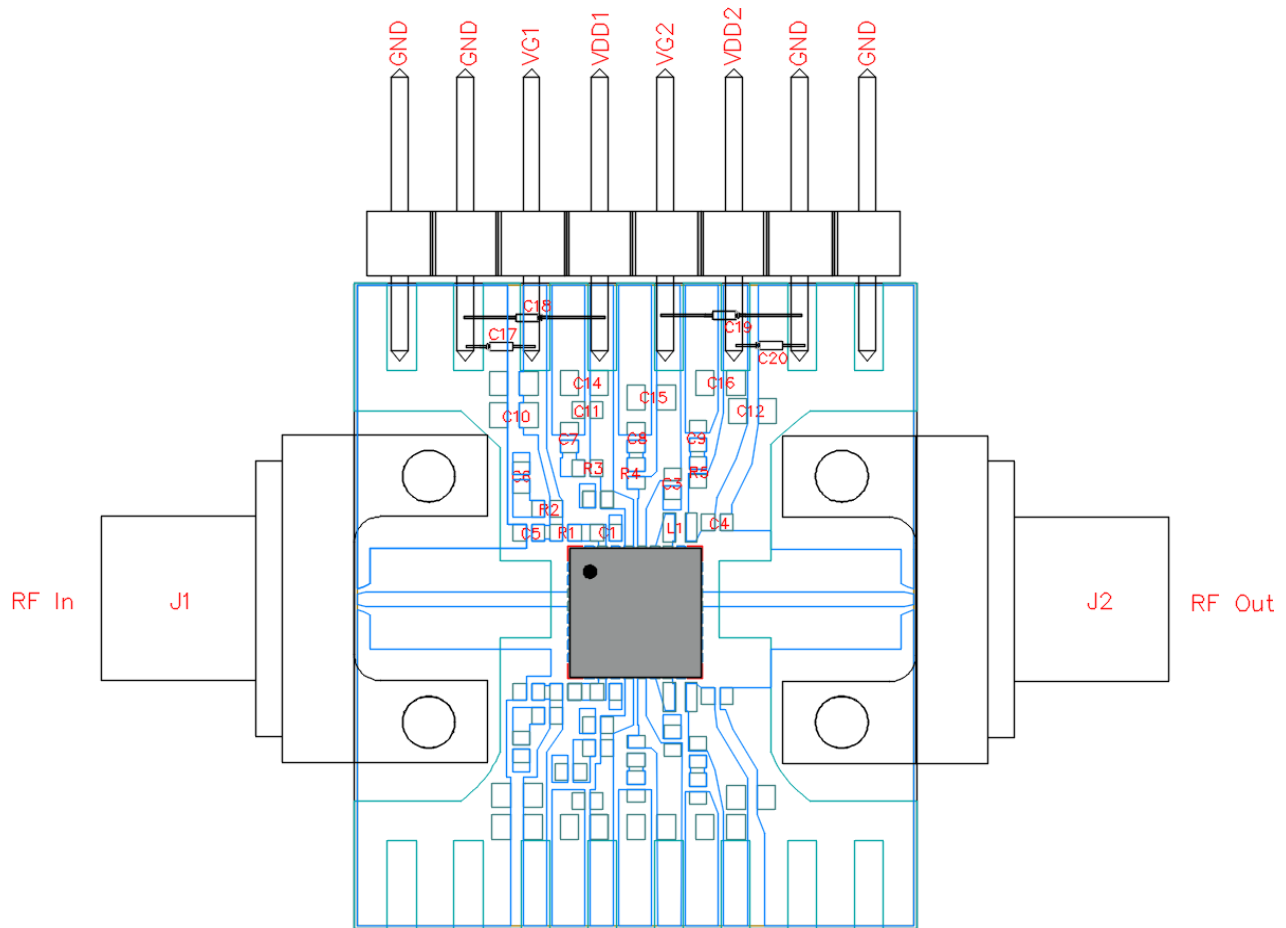


### TYPICAL RF PERFORMANCE

Test conditions unless otherwise noted:  $VDD1 = 12V$ ,  $VDD2 = 28V$ ,  $VG1 = -2.47V$ ,  $VG2 = -2.45V$ ,  $IDQ1 = 20mA$ ,  $IDQ2 = 100mA$ ,  $Ta = 25^{\circ}C$ ,  $Z0 = 50\Omega$ , Wifi source: 802.11 64QAM3/4



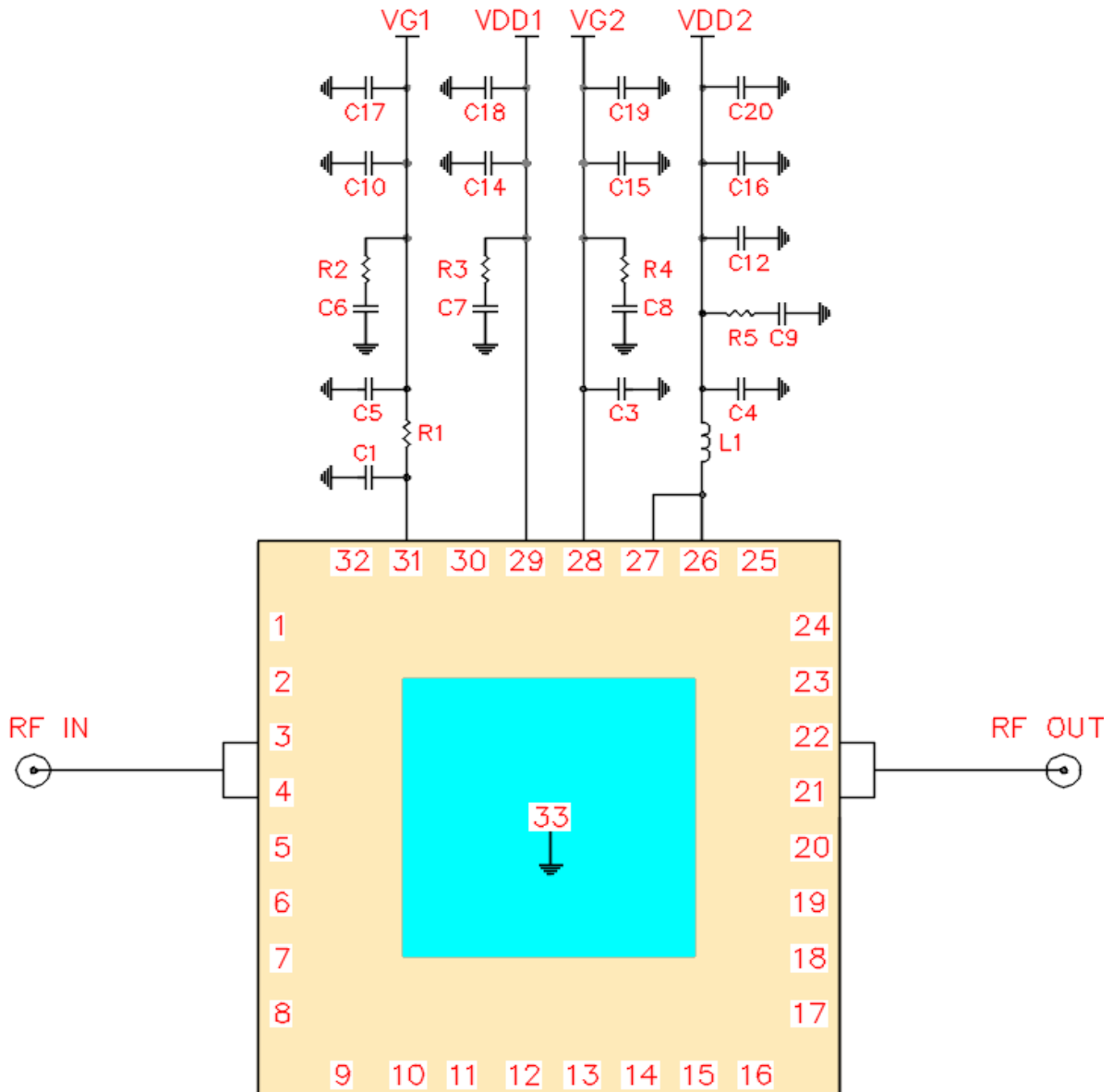
### Evaluation Board



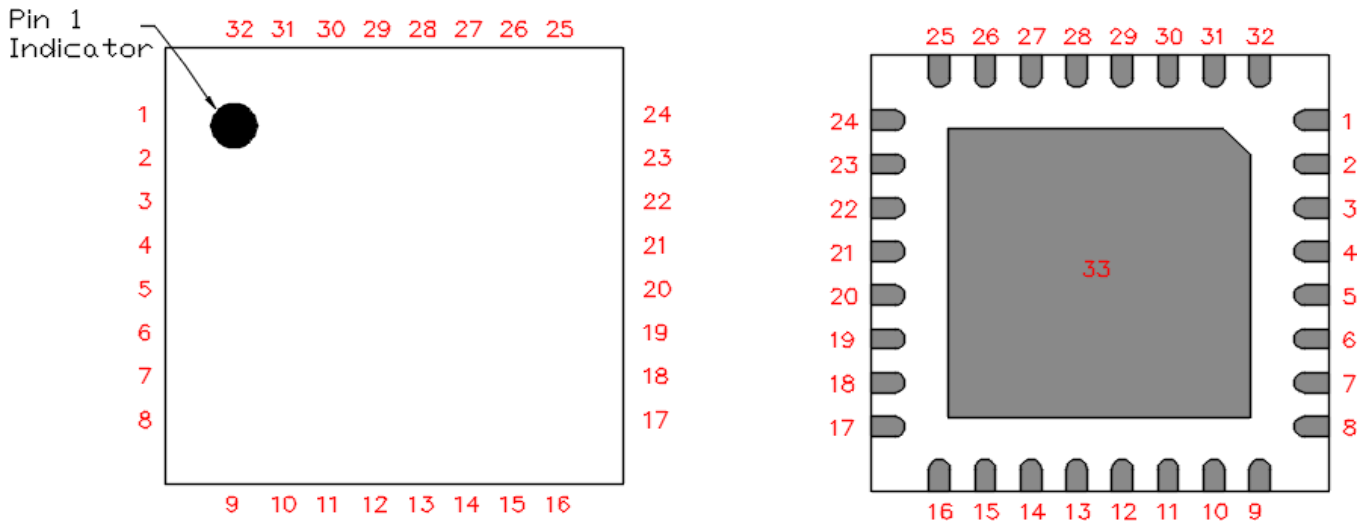
### Bill of Materials

| Reference          | Value   | Description                 | Manufacturer        | Part Number    |
|--------------------|---------|-----------------------------|---------------------|----------------|
| C1, C3, C9         | 5 pF    | CAP, 5%, 50V, NP0, 0402     | Various             |                |
| C4                 | 10 pF   | CAP, 5%, 50V, NP0, 0402     | Various             |                |
| C5, C8             | 100 pF  | CAP, 5%, 50V, NPO, 0402     | Various             |                |
| C6, C7, C15        | 1000 pF | CAP, 10%, 50V, X7R, 0402    | Various             |                |
| C10, C14, C16      | 1 uF    | CAP, 10%, 35V, X5R, 0603    | Various             |                |
| C11, C12           | 0.1 uF  | CAP, 10%, 50V, X8L, 0402    | Various             |                |
| C17, C18, C19, C20 | 1 uF    | CAP, 10%, 50V, TANT, AXIAL  | Various             | M39003/01-2356 |
| R1                 | 50 Ohm  | RES, 5%, 0.0625W, 0402      | Various             |                |
| R2, R3, R5         | 10 Ohm  | RES, 5%, 0.2W, 0402         | Various             |                |
| R4                 | 0 Ω     | RES, Jumper, 0402           | Various             |                |
| L1                 | 0.8 nH  | IND, 5%, 0402, Ceramic Chip | Coilcraft           | 0402DC-N80XJRW |
| J1, J2 (Connector) |         | SMA Female End Launch       | Southwest Microwave | 292-06A-6      |
| 03-50-225 (PCB)    |         | RO4350B, 0.254mm Thick      | Various             |                |

Schematic of Bias Circuit



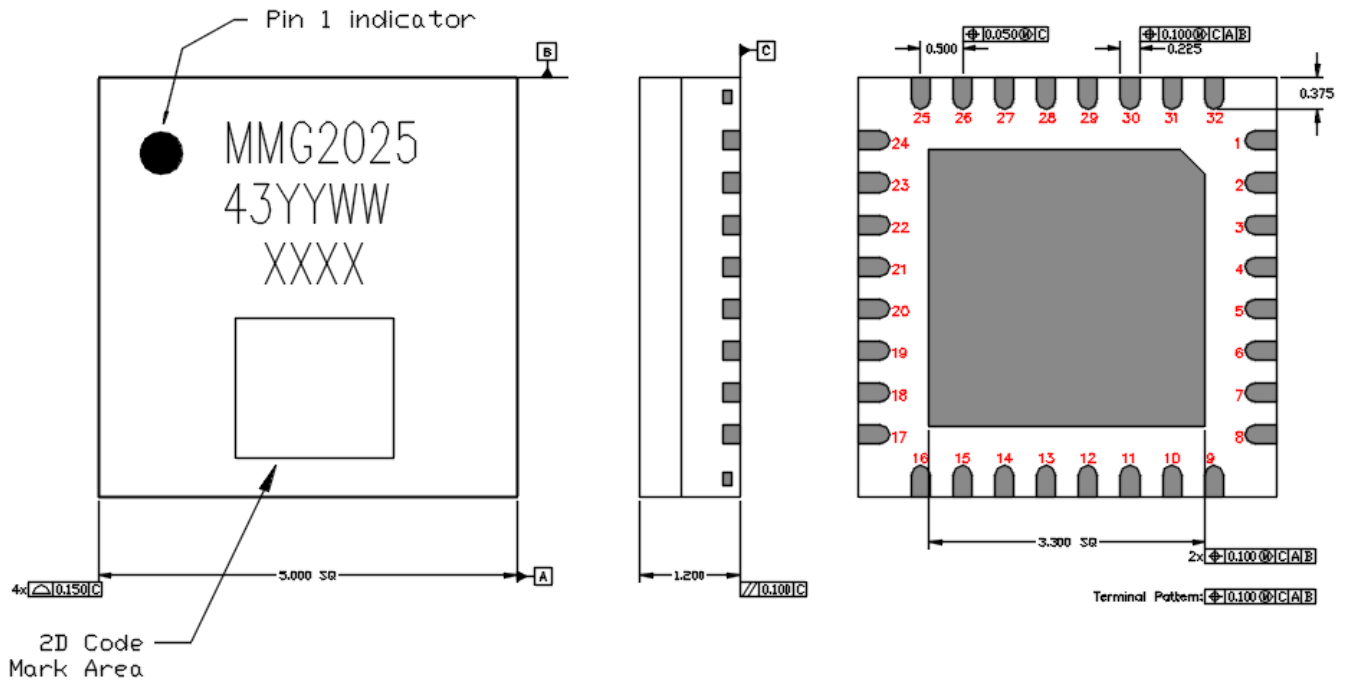
### Pin Layout



### Pin Description

| Pin Number            | Symbol | Description  |
|-----------------------|--------|--|
| 1, 2, 5-20, 23-25, 32 | NC     | No connection inside of package                        |
| 3, 4                  | RF IN  | RF input, 50 Ohms, DC blocked                          |
| 21, 22                | RF OUT | RF output, 50 Ohms, DC blocked                         |
| 26, 27                | VDD2   | Drain voltage of 2nd stage. Biasing circuitry required |
| 28                    | VG2    | Gate voltage of 2nd stage. Biasing circuitry required  |
| 29                    | VDD1   | Drain voltage of 1st stage. Biasing circuitry required |
| 31                    | VG1    | Gate voltage of 1st stage. Biasing circuitry required  |
| 33                    | GND    | Center ground  |

### Mechanical Information



#### Notes:

1. All dimensions are in millimeters
2. Markings:
  - Line 1: MMG2025
  - Line 2: 43YYWW: YY for the last two digits of the year and WW for the work week
  - Line 3: XXXX (Lot code)
  - Line 4: 2D code for XXXX (Lot code) from line 3
3. Plating of the Package
  - Ni: 0.5um. MIN.
  - Pd: 0.02um. MIN.
  - Au: 0.05um. MAX.

## Contact Information

For additional information please visit [www.cmlmicro.com](http://www.cmlmicro.com) or contact a sales office.

| Europe  | America  | Asia   |
|---|--|--|
| <ul style="list-style-type: none"><li>• Maldon, UK</li><li>• Tel +44 (0) 1621 875500</li><li>• <a href="mailto:sales@cmlmicro.com">sales@cmlmicro.com</a></li></ul> | <ul style="list-style-type: none"><li>• Winston-Salem, NC</li><li>• Tel +1 336 744 5050</li><li>• <a href="mailto:us.sales@cmlmicro.com">us.sales@cmlmicro.com</a></li></ul> | <ul style="list-style-type: none"><li>• Singapore</li><li>• Tel +65 6288129</li><li>• <a href="mailto:sg.sales@cmlmicro.com">sg.sales@cmlmicro.com</a></li></ul> |

Although the information contained in this document is believed to be accurate, no responsibility is assumed by CML for its use. The product and product information is subject to change at any time without notice. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with product specification.

© 2023 CML Microsystems Plc